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(54) Abstract Title

Data processing system with a dynamically adjustable channel framework

(57) A data processing system utilises a number of dynamically adjustable asynchronous data/address channels CH in place of a conventional synchronous data bus. A system controller 60 consisting of a control logic 62 and a switching box 61 receives the transmission requirements of a CPU 10, memory 30, peripheral devices 50 etc and sets-up appropriate channels to accommodate these requirements. For example, transmissions requiring a high bandwidth may be allocated several channels. The channel arrangements are adjusted in accordance with changes in the data flow, and each channel may be operated independently. The switching box may consist of a plurality of interconnected buffers and have various states depending on the channel settings, e.g. uni-directional, bi-directional or multi-channel settings (see figures 6-8). Activated channels follow a unique transmission direction in order to reduce turnover time when switching transmission direction.

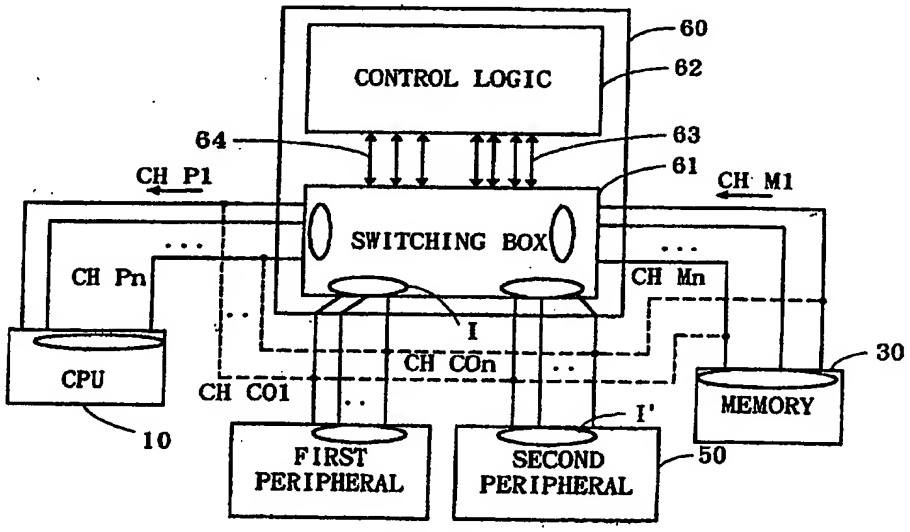

FIG. 3

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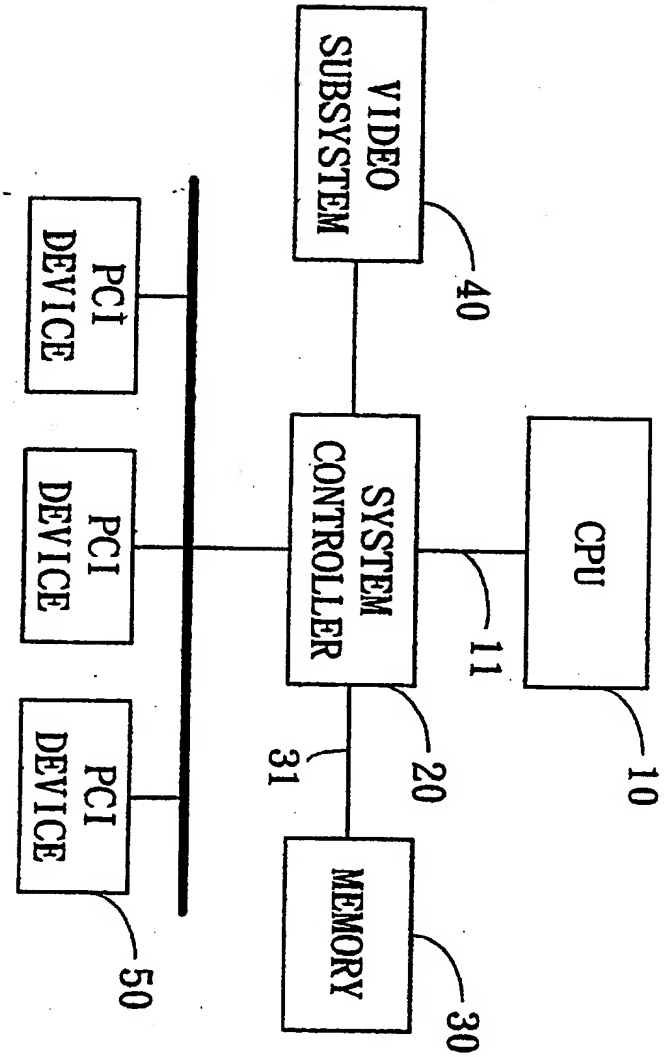
VIDEO SUBSYSTEM
40
PCI DEVICE
PCI DEVICE
PCI DEVICE
50
SYSTEM CONTROLLER
11
CPU
10
31
20
MEMORY
30

FIG. 1

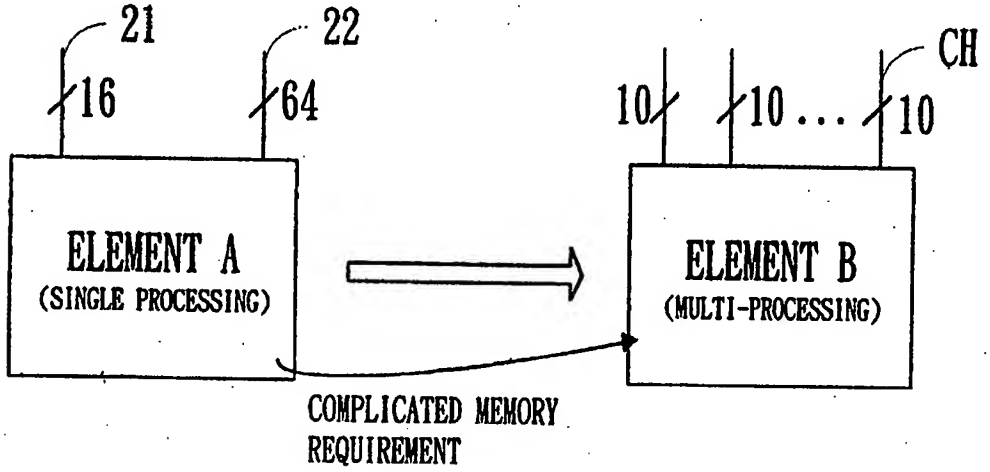
21
22
16
64
10
10 ...
10
CH
ELEMENT A
(SINGLE PROCESSING)
ELEMENT B
(MULTI-PROCESSING)
COMPLICATED MEMORY
REQUIREMENT

FIG. 2

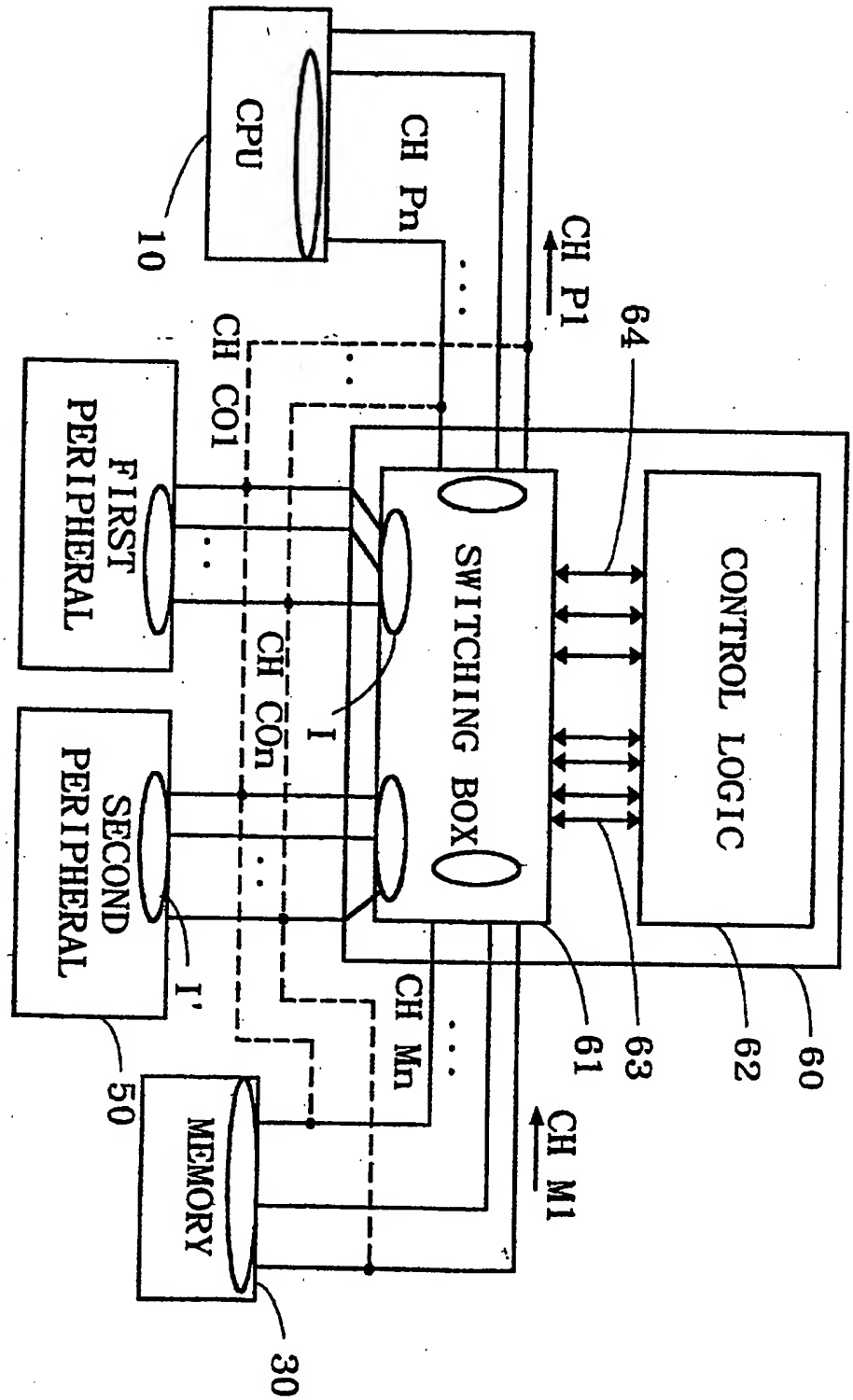
CPU
10
CH Pn
CH P1
64
CONTROL LOGIC
SWITCHING BOX
CH CO1
CH COn
I
FIRST PERIPHERAL
SECOND PERIPHERAL
I'
50
CH Mn
CH M1
61
63
62
60
MEMORY
30

FIG. 3

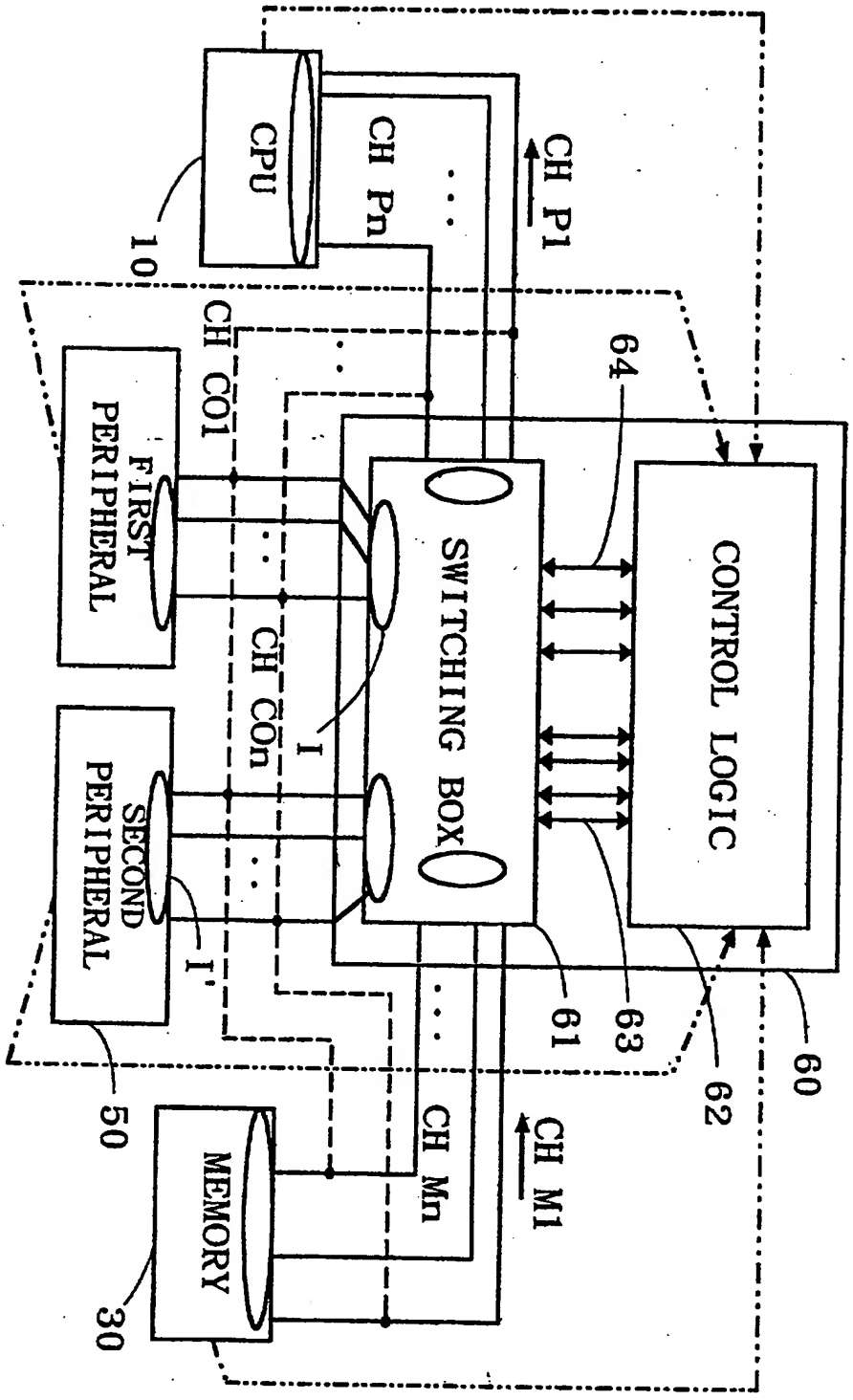
CPU
10
CH Pn
CH P1
CH CO1
CH COn
FIRST PERIPHERAL
SECOND PERIPHERAL
50
I
I'
SWITCHING BOX
64
CONTROL LOGIC
61
63
62
60
CH Mn
CH M1
MEMORY
30

FIG. 4

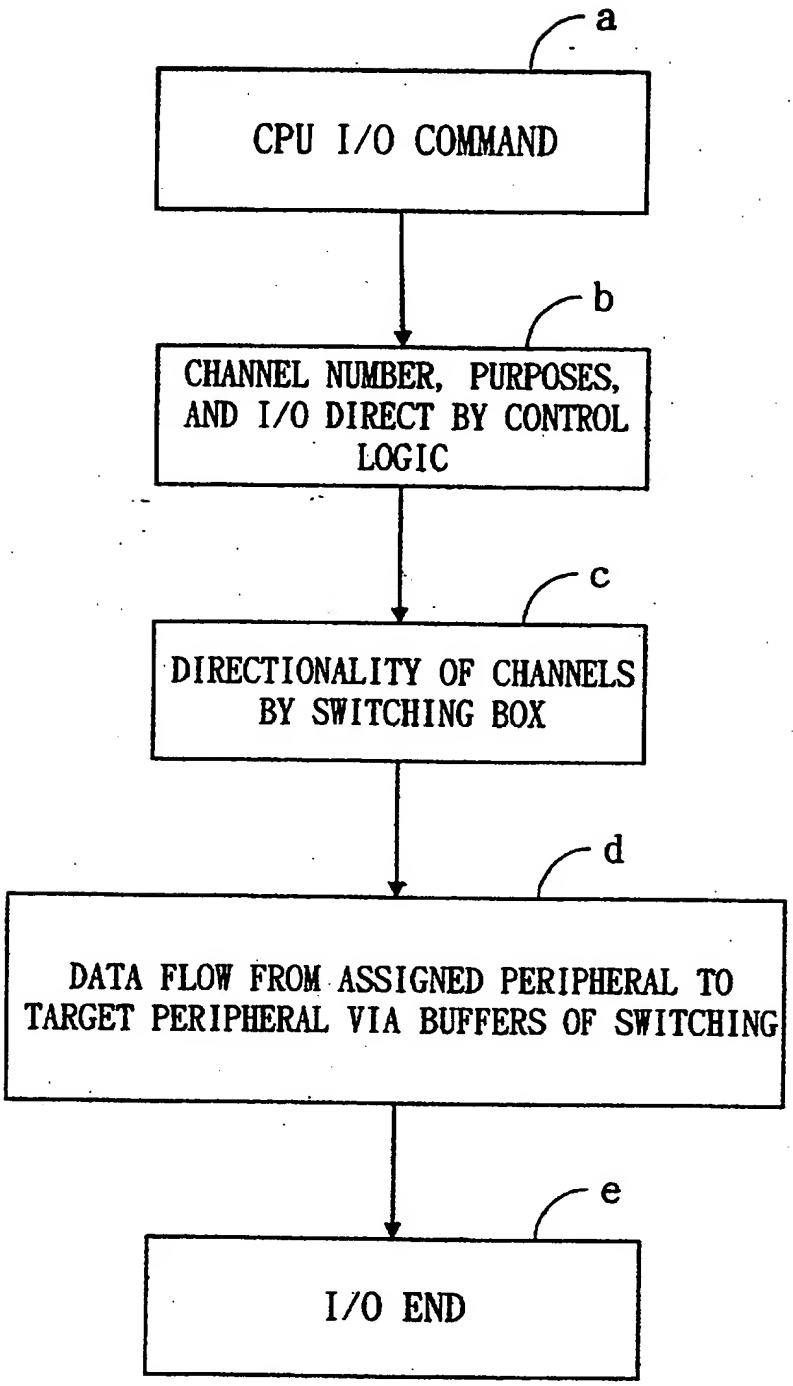
a
CPU I/O COMMAND
b
CHANNEL NUMBER, PURPOSES, AND I/O DIRECT BY CONTROL LOGIC
c
DIRECTIONALITY OF CHANNELS BY SWITCHING BOX
d
DATA FLOW FROM ASSIGNED PERIPHERAL TO TARGET PERIPHERAL VIA BUFFERS OF SWITCHING
e
I/O END

FIG. 5

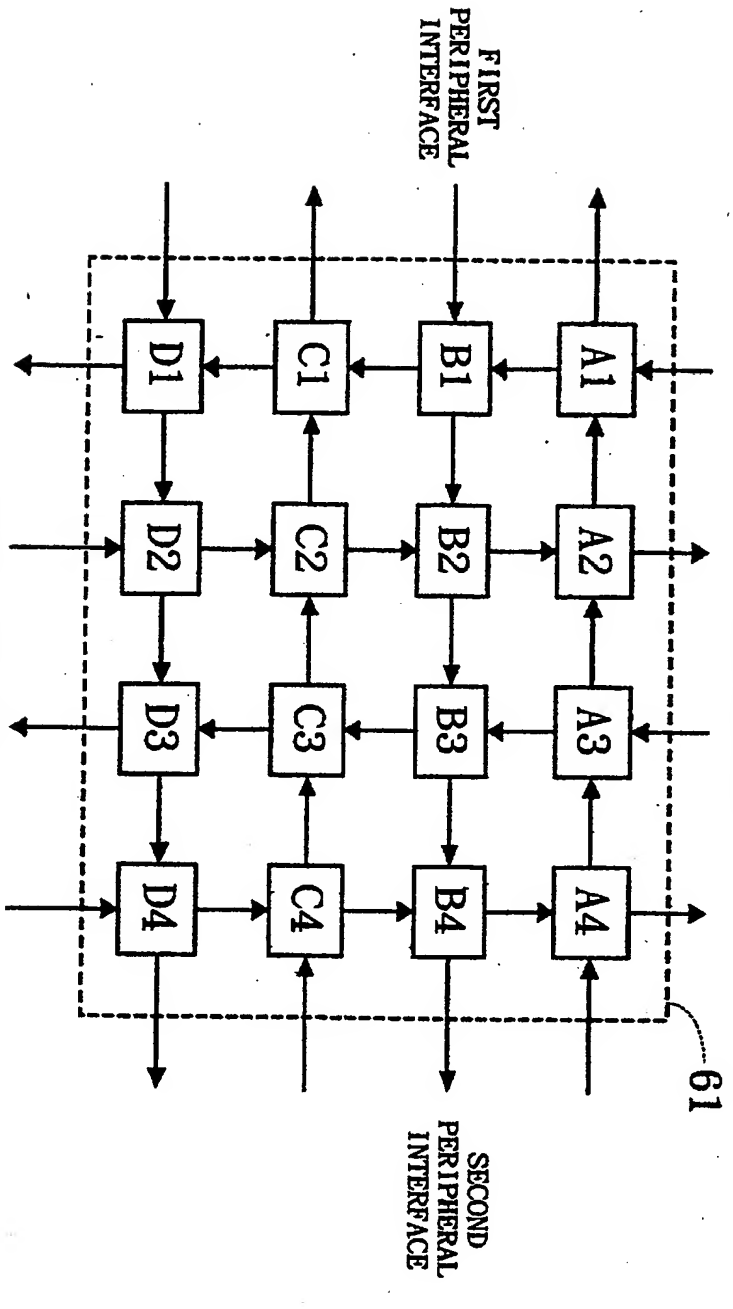
CPU INTERFACE
FIRST PERIPHERAL INTERFACE
SECOND PERIPHERAL INTERFACE
THIRD PERIPHERAL
A1
A2
A3
A4
B1
B2
B3
B4
C1
C2
C3
C4
D1
D2
D3
D4
61

FIG. 6

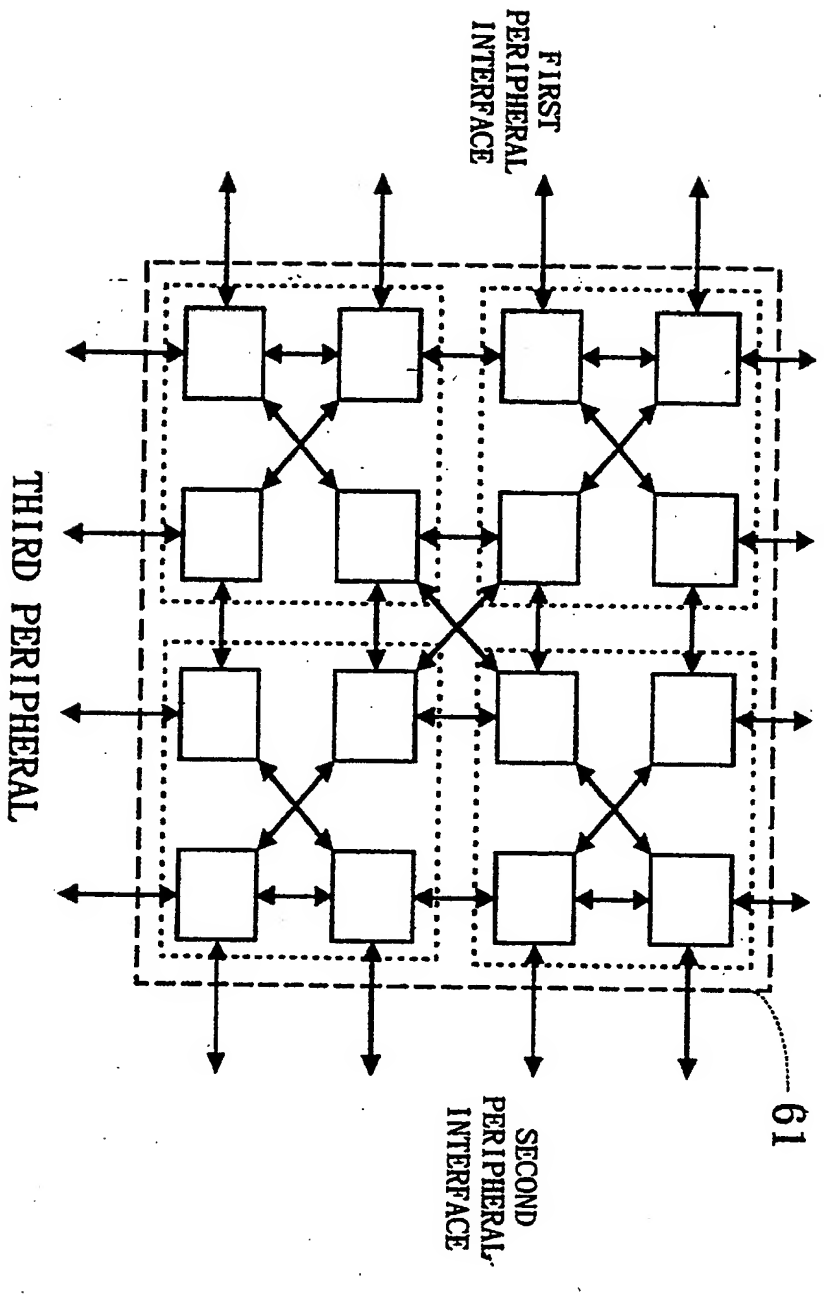
FIRST PERIPHERAL INTERFACE
CPU INTERFACE
THIRD PERIPHERAL
SECOND PERIPHERAL INTERFACE
61

FIG. 7

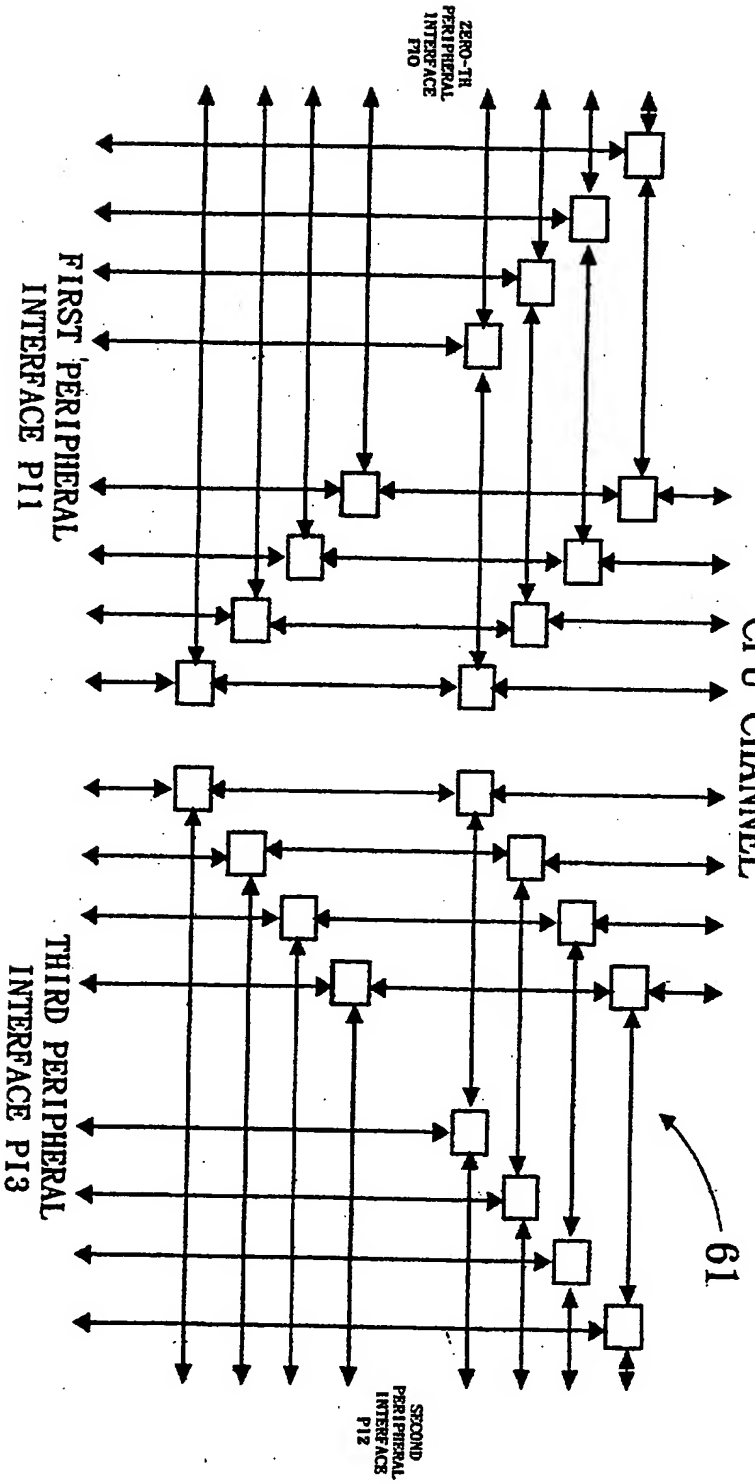
ZERO-TH PERIPHERAL INTERFACE PI0
FIRST PERIPHERAL INTERFACE PI1
CPU CHANNEL
THIRD PERIPHERAL INTERFACE PI3
SECOND PERIPHERAL INTERFACE PI2
61

FIG. 8

DATA PROCESSING SYSTEM WITH AN ADJUSTABLE DATA/ADDRESS CHANNEL FRAMEWORK

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a data processing system with an adjustable data/address channel framework, and more particularly to a data processing system which includes asynchronous data/address channels for replacing conventional synchronous data buses and which is capable of determining channel number and transmission bandwidths required between every two elements according to practical requirement upon data flow.

(2) Description of the Prior Art

Referring to FIG.1, a basic structure of a conventional computer system is shown. The computer system includes a central processing unit 10 (CPU), a system controller 20, a memory 30, a video subsystem 40, and a plurality of peripheral component interconnect (PCI) devices 50. The connection and transmission among aforesaid elements are usually established via buses with a plurality of signal I/O lines. The system controller 20 is utilized as a bridging interface between the CPU 10 and other system elements such as the memory 30, the video subsystem 40 and the PCI devices 50. For example in a conventional computer, the system controller 20 can be embodied as one of system chipsets or a north bridge. A system bus 11 for bridging the system controller 20 and the CPU 10 includes a plurality of parallel data I/O lines and address I/O lines. For example in a Pentium II computer or a PowerPC, it uses 64 data I/O lines and 32 address I/O lines to parallel receive or transmit data and address signals. In addition, a memory bus 31 for bridging the system controller

20 and the memory 30 includes 64 data I/O lines and a substantial number of address I/O lines (actual number of address I/O lines is dependent upon the type of the memory 30). Another feature of the conventional bus is its uniqueness. For example, when signals are transmitted from the memory 30 to the video subsystem 40, all data I/O lines and address I/O lines will be occupied for this specific transmission purpose. It is forbidden at the same time for the memory 30 to transmit any signal back to the CPU 10.

To simplify the description, aforesaid bus can have two following features.

1. Multiple parallel data/address lines: which contribute to the processing bandwidths required for transmitting data/address signals. For example, the bandwidth can be doubled by increasing the number of data lines from 32 to 64, with the same operational clock.
2. Uniqueness and synchronicity: which is advantageous in clearly defining the time sequences. Therefore, great convenience can be achieved during implementations, and the communication protocol across the bus can be easily established.

Though parallelization and synchronization are beneficial to the conventional bus, yet following shortcomings are also inevitable.

1. The development history of clock frequency is from 8 MHz, to 16 MHz, to 33 MHz, to 66 MHz, and finally now to 100 MHz. However, as the increase in the operational clock frequency, so does the difficulty in synchronization.
2. Currently, the bit width of data/address lines for the bus used in most computer systems is 64 bit. However, it can be foreseen that the 128 bit-width lines will become the main streams in the near future. The increase in bit width of data lines implies a substantial increase in pin count of an IC. In case of a big pin

count, the difficulty in IC packaging will be greatly increased and the size of the package will be increased as well. In the aforesaid elements, the system controller 20 is the most affected by the increase in pin count, due to its connection relationships in the conventional computer system.

3. Parallel data/address I/O lines will consume greater power and generate much noise at the moment of simultaneous switching from 0's to 1's, or from 1's to 0's.

4. The capacity of data flow manageable by the system controller 20 is limited and fixed. Therefore, even though the bit width can be increased by extending the pin count, the increase in overall performance can yet be assured. That is, it is highly possible that the less performance can be enhanced after increasing the pin count.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a data processing system with an adjustable data/address channel framework, which uses asynchronous data/address channels to replace conventional synchronous data buses. The system controller of the present invention utilizes a plurality of channels to transmit address/data between connected elements. By providing a switching box and a control logic to the system controller, connection status of channels among elements can then be determined. To achieve optimal data transmission, channel number and transmission bandwidths required between every two elements are determined according to practical requirement upon data flow.

In accordance with the present invention, the switching box, comprising a plurality of data buffers, has at least three states; that is, a state fixed-direction setting, a state of dynamic-direction setting, and a state

of multi-channel setting. The switching box can remain at any of aforesaid states, or at any other suitable variant state. By determining the control logic, the states of data buffers in the switching box can be properly adjusted to obtain suitable directionality of channel transmission in accordance with specific channel-connection requirement, and also a respective buffer area can be formed in the switching box.

Accordingly, each channel of the present invention can operate independently. A higher data transmission rate can be achieved by utilizing a larger number of channels. As the channel is constructed, its transmission direction is also fixed; so that turnover time can be reduced during transmission and thus overall transmission rate of the data processing system can be increased as well.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be specified with reference to its preferred embodiments illustrated in the drawings, in which

FIG.1 shows a basic structure for a conventional computer system;

FIG.2 illustrates schematically the differences between the present invention and the prior art;

FIG.3 shows a first embodiment of the data processing system in accordance with the present invention;

FIG.4 shows a second embodiment of the data processing system in accordance with the present invention;

FIG.5 is a flow chart for the data processing system in accordance with the present invention;

FIG.6 illustrates schematically a switching box as a fixed-direction setup type;

FIG.7 illustrates schematically a switching box as a dynamic-direction

setup type; and

FIG.8 illustrates schematically a switching box as a multi-channel setup type.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention disclosed herein is directed to a data processing system with an adjustable data/address channel framework. In the following description, numerous details are set forth in order to provide a thorough understanding of the present invention. It will be appreciated by one skilled in the art that variations of these specific details are possible while still achieving the results of the present invention. In other instances, well-known components are not described in detail in order not to unnecessarily obscure the present invention.

The framework of the present invention is provided to replace the aforesaid conventional buses by introducing adjustable data/address channel models. The comparison between the present invention and the prior art is shown in FIG.2.

In a bus framework of the prior art shown at the left portion of FIG.2, an element A (can be any of elements in FIG.1) uses a bus to connect with the system controller 20. Typically, the bus can have an address bus 21 (16 bits) and a data bus 22 (64 bits). Due to the uniqueness and the synchronization of the bus, the I/O request, read or write, for the memory 30 as an example is executed according to unique timing, unique memory, and a fixed address. For the element A itself, the situation is defined as a single processing.

According to the channel framework of the present invention, identical pin count can be used to construct several channels CH. Each channel CH can be adjusted in accordance with each respective requirement. That is, for example, different addresses can be read or written at the same time per

specific memory's requirement. By applying the aforesaid example in pin count, 8 channels CH can be constructed and each of the channels CH can includes 10 signal lines. By providing such an arrangement, an optimal channel combination can be constructed in accordance with practical needs to enable element B executing a multi-processing.

Accordingly, each channel CH can operate independently. A higher data transmission rate can be thus achieved by utilizing a larger number of channels CH. As the channel is constructed, its transmission direction is also determined; so that no more turnover time can exist during transmission to cause time delay. In addition, the ideas of channels CH and conventional signal lines are different. Each channel CH can have several signal lines, and each signal line transmits data in accordance with the transmission protocol of the channel. In the present invention, the transmission protocol of the channel CH itself is not specifically defined and can be varied to meet specific purpose. As the aforesaid example, 10 signal lines are used to construct a channel. Among these signal lines, one can be used as a clock line, one can be an address line for transmitting data sequentially, and eight can be assigned as data lines for parallel transmission. Nevertheless, the channel construction can be varied per practical requirements.

In the present invention, it is important to understand how the system controller 20 controls the channel CH and how to adjust the channel CH. Following are two embodiments to explain the details.

Referring now to FIG.3, a first embodiment of the present invention is shown. The system controller 60 acts as a channel manager, and each channel CH stands for a data flow with a fixed transmission rate between the system controller 60 and any external element as the CPU 10, the memory 30, or the peripheral. The system controller 60 includes a switching box 61 and a control logic 62. The switching box 61 can consist of a plurality of data buffers. According to the present invention, the switching box 61 can have various states; they are, a state of fixed-

direction setting, a state of dynamic-direction setting, a state of multi-channel setting, and any other state with respect to suitable setting. The purpose of the control logic 62 is to perform practical transmission control among elements, so that the switching box 61 constructed by the data buffers can be regulated. Thereby, practical channel CH can then be established between two external elements.

Refer now to FIG.3, especially focusing upon the channel CH P1 and the channel CH M1. When the CPU 10 reads data from the memory 30, the transmission direction along the channel CH M1 can be set from the memory 30 to the system controller 60, and the transmission direction along the channel CH P1 can be set from the system controller 60 to the CPU 10. The control logic 62 will generate a series of direction setting signals 63 and another series of switching control signals 64 in accordance with practical needs of the element, for controlling the action of each data buffer in the switching box 61. Thereby, the transmission channel of information (including both data and address) in between can be established. When an element transmits some signals to another element, following information need to be included.

1. Tag: to indicate the target element.
2. Data: to be forwarded.
3. Address: to index the address of the forwarded data at the target element.

In addition, the data to be transmitted might include a substantial portion of control signals. In the present invention, these data are transmitted through the constructed channels CH.

Further, in FIG.3, the elliptical marks between the system controller 60 and other elements represent the respective interface processing circuits I and I'. The data transmission in between needs to follow the same channel transmission protocol. One important thing to be noted is the

mobility of the channel arrangement provided by this present invention, by which the disadvantage of conventional bus framework can be improved.

While the system controller 60 controls the flow of address/data signals, the number of channels CH required is dependent on the practical data flow. That is, when the data flow of any element is enlarged, the system controller 60 will open more channels to increase the communication bandwidth for the element. Thereby, the data transmission of the element can be speeded up. It is obvious that the channel arrangement among elements under the framework in accordance with the present invention can be dynamically adjusted, though the total number of the channels is fixed. For the example shown in FIG.3, the system controller 60 connects with the CPU 10, the memory 30, the first peripheral and the second peripheral, via different channels. Also, several intersectional channels (shown as dashed lines in FIG.3) are constructed; for example, channels CH CO1 to CH COn that connects the CPU 10 to the first peripheral. During the signal transmission, the CPU 10 may use 8 channels CH to communicate with other elements. It is possible that 4 channels (said CH CO1 ~ CO4) might be used to communicate with the first peripheral per the huge transmission requirement in between, and the rest 4 channels are used for the communication requirement with all other elements. Thereby, the channels CH around the CPU 10 can be optimally arranged.

According to the present invention, each channel CH can only maintain a unique transmission direction while being activated. The address/data information transmitted inside the channel CH needs to follow a predetermined transmission format. By this arrangement, the turnover time for direction switching during transmission can be reduced and thereby the transmission speed can be increased consequently. One point to be noted is that one channel CH is not necessary to be synchronic with another channel CH. That is, each channel CH of the present invention can operate independently.

Referring now to FIG.4, a second embodiment of the present invention is present. Basically, the framework of the second embodiment is improved from the first embodiment of FIG.3. The major difference in between is the transmission of the tag and control signals. In FIG.3, the tag and control signals are transmitted via the channel itself. On the other hand, in FIG.4, a single pin symbolized by a dashed line labeled as control/tag is used to execute the transmission of the tag and control signals. Under such an arrangement, the complexity of time sequence for non-data information inside the channel can be reduced. However, the number of the pin count is increased at the same time.

Further, the second embodiment shown in FIG.4 also has the same mobility as the first embodiment shown in FIG.3.

According to aforesaid description of the present invention, the flow chart illustrated in FIG.5 can be used to explain further the transmission pattern of the present invention.

Step a. The CPU 10 issues an I/O command.

Step b. The control logic 62 inside the system controller 60 generates a series of direction setting signals 63 and a series of switching control signals 64 per the I/O command or other practical requirements, for controlling every motion of every data buffer inside the switching box 61. Thereby, a complete data transmission channel can be established. Wherein, aforesaid motion includes channel number, purposes and I/O directions.

Step c. The switching box 61 performs the switching of buffers per system setting for establishing the directionality of data transmission.

Step d. Data flows from an assigned peripheral to a target peripheral via the channel composed of buffers.

Step e. The I/O job is over.

As stated previously, the switching box 61 comprises a plurality of

data buffers. In the following description, three types of setups are introduced to elucidate the motion of the switching box 61.

Referring now to FIG.6, a fixed-direction setup of the switching box 61 is shown. In this setup, data buffers inside the switching box 61 are all unique-direction devices. For example, the data buffer A1 has two data-coming directions; one from the CPU interface and another from the adjacent data buffer A2. Also, the data buffer A1 has two outgoing directions; one directing to the first peripheral (as the video subsystem 40 of FIG.1) and another directing to the adjacent data buffer B1. Therefore, in order to construct a channel CH from the CPU 10 to the third peripheral (as the memory 30 of FIG.1), two routes in FIG.6 can be selected; that is, one as A1-B1-C1-D1 and another as A3-B3-C3-D3. On the other hand, to construct the channel from the third peripheral to the CPU interface, both route D2-C2-B2-A2 and route D4-C4-B4-A4 can be selected. The advantage from using this fixed-direction setup upon the switching box 61 is the simplicity in frameworking, by which the embodiment can be easily constructed. Yet, the efficiency of using data buffers in this type of setup is not obvious.

Referring now to FIG.7, a dynamic-direction setup of the switching box 61 is shown. In this setup, the connection lines around any data buffer are all bi-directional and adjustable. That is, the transmission direction of every connection line is predetermined by the control logic 62. Though every connection line is bi-directional, yet the uniqueness of the connection line is still maintained as long as the channel CH is set to operate. Thereby, the turnover time can be avoided. Due to the need of efficient resource allocation and higher complexity of performing bi-directional connection while applying the dynamic-direction setup, the cost of this embodiment is higher than that for the fixed-direction setup. Yet, the advantage of using the dynamic-direction setup is the increase in usage efficiency.

Referring now to FIG.8, a multi-channel setup of the switching box 61

is shown. In this setup, the connection lines around any data buffer are also all bi-directional. However, not all the data buffers can be arbitrarily allocated. In FIG.8, the data buffers located at the left half can only be allocated to the CPU channel, and to the channels located between the zero-th peripheral interface PI0 and the first peripheral interface PI1. On the other hand, the data buffers located at the right half can only be allocated to the CPU channel and channels between the second peripheral interface PI2 and the third peripheral interface PI3. In addition, in the multi-channel setup shown in FIG.8, the number of channels are substantially larger than the number of data buffers.

According to the present invention, the switching box 61 is consisted of data buffers and can have any of the above three setups, or other suitable setup. Through the setting of the control logic 62, the data buffers inside the switching box 61 can be adjusted to any channel CH setup for constructing the directionality of channel transmission, in accordance with the requirement of channel connection. Also, a buffer area within channels can thus be formed.

As stated, the data processing system with an adjustable data/address channel framework in accordance with the present invention can use a plurality of channels to transmit address/data signals. By providing the switching box and the control logic to the system controller, channel connection among elements can thus be established. The required channel number as well as the transmission bandwidth between two elements can be determined in accordance with the practical requirement of data flow. The optimal data transmission can then be achieved. It is obvious that the present invention provides a resolution to the disadvantage of conventional bus framework with a single processing.

While the present invention has been particularly shown and described with reference to preferred embodiments, it will be understood by those skilled in the art that various changes in form and detail may be without departing from the spirit and scope of the present invention.

I claim:

1. A data processing system with an adjustable data/address channel framework, comprising elements such as a CPU, a memory and a plurality of peripheral devices, including a system controller connecting with the elements via a plurality of independent-operated channels for transmitting data and address signals, characterized in that: the system controller includes therein a switching box and a control logic, the control logic receives transmission requirements from the elements and determines a setup of the switching box for establishing a mutual-communication channel, and both channel arrangement and the setup are capable of being mobile adjusted per respective data transmission flow.

2. The data processing system with an adjustable data/address channel framework according to claim 1, wherein said control logic is used to generate a series of direction setting signals and a series of switching control signals per practical transmission requirements of any said element, for controlling operation of said switching box.

3. The data processing system with an adjustable data/address channel framework according to claim 1, wherein said elements transmit signals including a tag signal to indicate a target element, data signals, and address signals at the target element.

4. The data processing system with an adjustable data/address channel framework according to claim 1, wherein said switching box includes a plurality of data buffers to form a setup type as a fixed-direction setup, a dynamic-direction setup, a multi-channel setup, or other suitable setups.

5. The data processing system with an adjustable data/address channel framework according to claim 4, wherein said fixed-direction setup implies that each said data buffer is single-directional and said data buffers with the same transmission direction are connected to form a

channel of data transmission.

6. The data processing system with an adjustable data/address channel framework according to claim 4, wherein said dynamic-direction setup implies that every connection line around each said data buffer is bi-directional and adjustable, and a direction of each said connection line is predetermined by said control logic during said channel arrangement.

7. The data processing system with an adjustable data/address channel framework according to claim 4, wherein said multi-channel setup implies that every connection line around each said data buffer is bi-directional, and every said data buffer is allocated to a channel connected to said adjacent element.

8. The data processing system with an adjustable data/address channel framework according to claim 1, wherein said channel maintains unique transmission direction while being activated, and said data/address signals transmitted in said channel follow a predetermined transmission format for saving turnover time upon direction switching.

9. The data processing system with an adjustable data/address channel framework according to claim 1, further includes interface processing circuits to respective said channels between said system controller and said elements, any data transmission therebetween following a same channel transmission protocol.

10. The data processing system with an adjustable data/address channel framework according to claim 1, wherein said each channel includes a plurality of signal lines following a same channel transmission protocol to transmit signals.

Application No: GB 0025565.3 **Examiner:** Matthew Nelson
Claims searched: 1-10 **Date of search:** 21 June 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): G4A (AFGDC, AFN); H4P (PFD, PPBC, PPK, PX)

Int Cl (Ed.7): G06F 13/14, 13/36, 13/362, 13/38, 13/40; H04L 12/403, 29/06

Other: Online: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	WO 96/41274 A1	(ADVANCED MICRO DEVICES) See whole document.	1-3 & 8-10
A, P	US 5991824	(STRAND et al) See e.g. col. 3, line 58 - col. 4, line 16; col. 8, lines 1-24; col. 9, lines 4-41; col. 12, lines 30-34 and figures 8-12.	
A	US 5790815	(SWANSTROM & BELT) See col. 4, lines 16-33 and 49-60; col. 18, lines 46-56 and col. 19, line 51 - col. 20, line 3.	
X	US 5734843	(GEPHARDT et al) See whole document.	1-3 & 8-10
A	US 4604743	(ALEXANDRU) See col. 2, lines 10-22, 43-60 and col. 6, lines 53-64.	
A	US 4075608	(KOENIG) See e.g. the abstract.	

X Document indicating lack of novelty or inventive step
Y Document indicating lack of inventive step if combined with one or more other documents of same category.
& Member of the same patent family
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E Patent document published on or after, but with priority date earlier than, the filing date of this application.